CLAIM OBJECTIONS

Claim 8 is objected to for various formalities cited by the Examiner. Applicant has amended Claim 8 accordingly. However, Applicant has amended claim 8 for clarification purposes only. No modification in claim scope or range of equivalents is intended through these changes. Withdrawal of the rejection is therefore respectfully requested.

35 USC § 103 Rejection

The Examiner rejects Claims 1-8 under 35 USC §103 as being unpatentable over Hisao et al (JP 10209467). The Examiner states that Hisao discloses a gate electrode having a thickness of about 100 nm which could be more or less than 100 nm. The Examiner states that, therefore, the thickness of the gate electrode disclosed in Hisao reads on the Claims. The Examiner further states that because the general conditions of the claim are disclosed, it would be obvious to one of ordinary skill in the art to modify Hisao to the less than 100 nm range disclosed by Applicant. Applicant respectfully traverses this rejection.

Hisao fails to disclose the specific range limitation as disclosed in the present application. In fact, from reviewing Hisao it is unclear whether any range for the gate electrode is disclosed. However, if the Examiner's reading is correct, then Hisao discloses a gate electrode thickness of 100 nm which does not overlap with Applicant's claimed range of less than 100 nm. This is in accord with the discussion provided in the background of the present application, in which the conventional state of the art includes gate thicknesses of greater than or equal to 100 nm. Hisao, like the present state of the art, does not disclose a gate thickness of less than a 100 nm.

The present application, contrarily, is directed to providing a gate thickness that is less than 100 nm. This range yields unexpected results not contemplated in Hisao. In fact, Applicant's determination of this range and the corresponding unexpected results prompted the filing of the present application. Accordingly, independent Claims 1 and 5 claim maintaining a gate thickness of *less* than 100 nm. Reviewing the specification, (beginning Page 7, line 24, for example), the conventional gate structured transistors (such as Hisao) are 100 nm or more. By reducing the thickness of the gate electrode to below 100 nm, as in the present invention, the thermal capacity of the gate electrode is reduced to thereby allow the gate to more closely follow the temperature of the insulating substrate. This expands the process margin during laser anneal and alleviates level differences to thereby suppress

pinhole formation. These features are unexpected and render an advantage not contemplated by the prior art. Therefore, the claimed range is an un-obvious modification which yields unexpected results over the cited art. See *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990); MPEP 2144.06. Moreover, as Hisao fails to disclose the cited range, it fails to teach or suggest every element and limitation as claimed in the present application. Accordingly, Applicant respectfully requests reconsideration of the rejected claims, and submits that independent Claims 1 and 5 and all claims depending therefrom are in condition for allowance.

CONCLUSION

For at least the above reasons, Applicants respectfully submits that the present invention, as claimed, is patentable over the prior art. If the Examiner has any issues which he believes can be expedited by a telephone conference, he is encouraged to telephone the undersigned Representative. All objections and rejections having been addressed, it is respectfully submitted that the present application is in condition for allowance, and a Notice to that effect is earnestly solicited. It is believed that any additional fees due with respect to the filing of this paper should be identified in any accompanying transmittal. However, if any additional fees are required in connection with the filing of this paper that are not identified in any accompanying transmittal, permission is given to charge Deposit Account 18-0013 in the name of Rader, Fishman & Grauer PLLC.

Respectfully submitted,

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By: _____

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MARKED-UP CLAIMS

1. A thin film semiconductor device comprising:

an insulating substrate; and

a thin film transistor formed on said insulating substrate, wherein

said thin film transistor is formed in a bottom gate structure having gate electrode, a gate insulating film, and a semiconductor thin film stacked in the order from below upward, and

said gate electrode is made of metallic material having a thickness of less than 100nm.

2. The thin film semiconductor device according to Claim 1, wherein

said gate insulating film has a thickness thicker than the thickness of said gate electrode.

3. The thin film semiconductor device according to Claim 1, wherein

said semiconductor thin film comprises polycrystalline silicon crystallized by an irradiation of a laser beam.

4. The thin film semiconductor device according to Claim 1, wherein

said gate electrode has a multi-layered structure stacked with an upper layer having comparatively low heat conductivity and high electric resistance, and a lower layer having comparatively high heat conductivity and low electric resistance.

5. A display device comprising:

an insulating substrate;

pixels arranged in a matrix form; and

thin film transistors for driving said respective pixels, whereinsaid pixels and said thin film transistors are formed as integrated circuits on said insulating substrate, each of said thin film transistors has a bottom gate structure having a gate electrode, a gate insulating film and a semiconductor thin film stacked in the order from below upward, and

said gate electrode is made of metallic material having a thickness of less than 100nm.

6. The display device according to Claim 5, wherein

said gate insulating film has a film thickness thicker than the thickness of the gate electrode.

7. The display device according to Claim 5, wherein

said semiconductor thin film comprises polycrystalline silicon crystallized by an irradiation of a laser beam.

8. (Amended) The display device according to Claim 5, wherein

said gate [electrodes have] <u>electrode has</u> a multi-layer structure stacked with an upper layer having comparatively low heat conductivity and high electric resistance, and a lower layer having comparatively high heat conductivity and low electric resistance.